In the Specification:

Please replace paragraph with new marked up paragraphs as shown below. Marked up copies of the amended paragraphs illustrating the changes are shown below.

Page 4, lines 7-11

B1 Figures 12B-16B show a first cross-section along lines b-b' ~~X-X'~~ (represented in Figure 12A) in each of the corresponding figures 12A-16A and 12C-16C; and

Figures 12C-16C show a cross-section along line c-c'~~Y-Y'~~ (represented in Figure 12A) in corresponding Figures 12A-16A and 12C-16C.

Page 9, lines 7-9

B2 Following the polysilicon fill step, as shown in Figures 7A-7C, a second nitride layer 155~~150~~ is deposited on the surface of the device wafer 102 to cover the trench area and the polysilicon in the trench.

Page 11, lines 3-7

B3 Finally, as shown in Figure 10 A-C, a TEOS oxide may be deposited into the area 160 which has been etched away by the polysilicon etch described with respect to Figure 8 and polished back to the nitride layer 150. The resulting device has gate impurity which is the same species as the source and drain.

Page 11, line 20 through page 12, line 4

B4 This process for fabricating the device of Figure 11 is shown in Figures 12A-C to Figures

16A-C. The device in Figure 12A-C represents the device processed up to the point shown in Figure 3A-C (following the device layer etch of Figure 3 A-C), but with the exposed (trench) areas filled with TEOS 210. TEOS 210 may be deposited in accordance with well-known techniques such that an upper surface of the TEOS layer reaches the upper surface of nitride 110.